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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,802	08/04/2004	Amy J. Gottsche	BUR920030165US1	4801

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,802	GOTTSCHE ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08042004, 08092004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Drawings

2. The drawings are objected to because descriptive labels other than numerical are needed for Fig. 1. See 37 CFR 1.84(o).

3. Figure 1 is objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "30" has been used to designate both "Pin Type" box in vector 1, 12, segment 24 and "Function Control" box in segment 22. It would appear that the "Pin Type" box in vector 1, 12, segment 24 should be changed to "36" in order to be consistent with vectors 14 and 16.

4. The drawings are objected to because of insufficient margins. See 37 C.F.R. § 1.84(g).

5. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 2 and 3 are objected to because of the following informalities: Limitation "a first initial vector" should be "the first initial vector. Appropriate correction is required.

7. Claim 3 is objected to because of the following informalities: Limitation "at least one of running a vector, delaying a vector, rerunning a vector, looping a vector" should be "at least one of running a vector, delaying a vector, rerunning a vector [or] looping a vector". Appropriate correction is required.

8. Claim 12 is objected to because of the following informalities: In "comprising;" the semicolon ";" should be changed to a colon ":". Appropriate correction is required.

9. Claim 18 is objected to because of the following informalities: The limitation "at least one of any one of" is a garbled phrase. This should read "at least one of". Also, "and offsetting" should be changed to "or offsetting". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Gruodis et al. (US-6092225), hereinafter Gruodis.

Claim 1 and 19:

Gruodis teaches defining a first initial vector (**a set of four vectors at the start of each cycle**) and defining at least one segment within the first initial vector (A test is organized into a succession of test cycles with **each test cycle being subdivided into four segments**). (Col. 3, ll. 49-62). Gruodis also teaches offsetting the first initial vector a predetermined amount (**vector alignment circuit 30**) within the at least one segment. (Col. 3, ll. 56-60, col. 5, ll. 22-32, col. 11, ll. 30-45). Gruodis further teaches defining a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop, defining a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector and coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test. (Col. 4, l. 10 to col. 6, l. 51).

Claim 2:

Gruodis teaches selecting a predefined vector pattern. (Col. 4, ll. 10-14).

Claim 3:

Gruodis teaches defining a first initial vector further comprises at least one of running a vector, delaying a vector, rerunning a vector [or] looping a vector. (Col. 4, l. 10 to col. 6, l. 51).

Claim 4:

Gruodis teaches overriding the first initial vector with a second vector. (Col. 8, ll. 21-24).

Claim 5:

Gruodis teaches selecting an input pin on a device to be tested for the first initial vector. (Col. 3, ll. 49-52).

Claim 6:

Gruodis teaches defining a name for the input pin on the device to be tested (**Tester 10 includes a set of J tester channels CH1 through CHJ, each connected to a separate pin of an integrated circuit device under test (DUT) 12**). (Col. 3, ll. 49-52, col. 13, l. 55 to col. 14, l. 21).

Claim 7:

Gruodis teaches defining a counter, and looping the first initial vector a prescribed number of times in accordance with the counter. (Col. 4, l. 10 to col. 6, l. 51).

Claim 8:

Gruodis teaches defining a data control vector to allow a prescribed input format of the first initial vector. (Col. 4, l. 10 to col. 6, l. 51).

Claim 9:

Gruodis teaches defining a new format vector to be added to the first initial vector to reconfigure the shape of the first vector. (Col. 4, l. 10 to col. 6, l. 51).

Claim 10:

Gruodis teaches defining a second vector, allocating a second segment configured to contain the second vector and offsetting the second vector a predetermined amount within the second segment. (Col. 3, ll. 49-62, col. 3, ll. 56-60, col. 5, ll. 22-32, col. 11, ll. 30-45, col. 4, l. 10 to col. 6, l. 51).

Claim 11:

Gruodis teaches defining a counter loop comprising loops of the second vector within the second segment to produce a second set of vectors having a prescribed number of vectors in accordance with the counter loop defining a progressively changing variation of the second vector for each loop of the counter loop so at least one vector of the second set of vectors varies from the second vector and outputting the second segment having the second set of vectors as per the rejection of claim 1 is repeated via the looping commands. (Col. 4, l. 10 to col. 6, l. 51).

11. Claims 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Theodoseau (US-5872797A), hereinafter Theodoseau.

Claim 12:

Theodoseau teaches selecting a macro definition file (**read macro 406, write macro 404**) defining at least one vector, forming a control bit definition file (**counter control 402**) configured to be added to the at least one vector, creating a pattern definition file (**pattern control selector 420**) configured to selectively alter a portion of the at least one vector, creating a global definition file (**refresh macro 408 includes write array, read array and variable retention testing**) configured to alter the entire vector and combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern (**The macros then build a plurality of patterns which are stored in memory 430 and read out in sequence, when called**). (Col. 6, l. 36 to col. 9, l. 50).

Claim 13:

Theodoseau teaches repeating the final pattern in accordance with a counter range. (Col. 7, ll. 39-51, Fig. 5).

Claim 14:

Theodoseau teaches forming setup vector files (**start-up vectors 414**) configured to power-up a device under test. (Col. 7, ll. 9-38, col. 11, ll. 49-58).

Claim 15:

Theodoseau teaches forming stability vectors files (**stability vectors 412**) configured to stabilize a device under test between actual test signals. (Col. 7, ll. 9-38, col. 11, ll. 49-58).

Claim 16:

Theodoseau teaches outputting the final pattern to a device under test. (Col. 6, l. 36 to col. 9, l. 50).

Claim 17:

Theodoseau teaches creating multiple final patterns and adding the multiple final patterns to one another. (Col. 19, l. 49 to col. 11, l. 40).

Claim 18:

Theodoseau teaches at least one of any one of overlapping, delaying, mixing, and offsetting at least two of the multiple final patterns. (Col. 6, l. 36 to col. 9, l. 50).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Huott et al. (US-6314540) teaches a substantial portion of the claims particularly partitioning test patterns into sub-sets of patterns (segmenting) and using seed vectors (initial vector).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr.
Examiner
Art Unit 2138

9/8/06

GUY LAMARRE
PRIMARY EXAMINER